REMARKS

The Official Action mailed January 22, 2003, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for Two Month Extension of Time*, which extends the shortened statutory period for response to June 22, 2003. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on October 31, 2000; January 30, 2001, February 5, 2002, and November 6, 2002. The Applicants also note the corrections of the IDS filed October 31, 2000. A further IDS is submitted herewith and careful review and consideration of this IDS is requested.

Claims 1-3 and 35-51 were pending in the present application. Claims 1 and 25-45 have been amended to better recite the features of the present invention and to correct minor typographical errors. New dependent claims 52-61 have been added to recite additional protection to which the Applicants are entitled. Claims 1-3 and 35-61 are now pending in the present application, of which claims 1 and 35-45 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 3 of the Official Action rejects claims 1-3, 35, 40, 43, 46 and 49 as obvious based on the combination of U.S. Patent No. 5,728,259 to Suzawa et al., U.S. Patent No. 5,306,651 to Masumo et al., and U.S. Patent No. 5,661,056 to Takeuchi. Paragraph 4 of the Official Action rejects claims 36, 38, 41, 44, 47, and 50 as obvious based on the combination of Suzawa, Masumo, Takeuchi, U.S. Patent No. 5,535,471 to Guldi, and Wolf, "Silicon Processing for the VLSI Era," Vol. 2, Chapter 4, last paragraph of p. 274 (1990). Paragraph 6 of the Official Action rejects claims 37, 39, 42, 45, 48 and 51 as obvious based on the combination of Suzawa, Masumo, Takeuchi, and U.S. Patent No. 4,759,610 to Yanagisawa. The Applicants respectfully submit that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present invention, as amended.

As stated in MPEP §§ 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available

to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Suzawa, Masumo, Takeuchi, Guldi, Wolf and Yanagisawa do not teach or suggest either performing a plasma treatment to the semiconductor island or forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride, and forming a resin material layer over the interlayer insulating film.

Amended independent claims 1, 36-39, and 41-45 recite the feature of performing a plasma treatment to the semiconductor island. Organic substances existing on the surface of the semiconductor island may be removed by the plasma treatment (please see p. 24, lines 9-21 and p. 25, lines 1-2 of the present specification.) Suzawa teaches away from this feature of the present invention in that Suzawa is directed to a "plasma-free process such as heated CVD" (abstract). Masumo, Takeuchi, Guldi, Wolf and Yanagisawa do not cure the deficiencies in Suzawa in that they are relied upon to teach a single or multilayer of silicon oxide or silicon oxide nitride, depositing silicon oxide nitride with TEOS, depositing silicon oxide nitride using N_2O, and TFT devices with an organic material (see, for example, pp. 5 and 8, Paper No. 20). Suzawa, Masumo, Takeuchi, Guldi and Wolf do not teach or suggest, either alone or in combination, performing a plasma treatment to the semiconductor island.

With respect to claims 35, 37, 39, 40, 42 and 45, the Official Action concedes that Suzawa "fails to teach forming a resin material layer over the interlayer insulating film 611" (p. 7, Paper No. 20). Although Yanagisawa discloses that a resin material insulating layer is used as the insulating film between the light shielding layer and the display pixel electrode, Suzawa and Yanagisawa, either alone or in combination, do not teach or suggest forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride, and forming a resin material layer over the interlayer insulating film. The above-recited arrangement of the present invention allows enhancement of the durability of the TFT by preventing infiltration of movable ions and moisture (please see p. 37, lines 12-17 of the present specification). Suzawa and Yanagisawa do not disclose the claimed arrangement of the present invention. Masumo, Takeuchi, Guldi and Wolf fail to cure the deficiencies in Suzawa and Yanagisawa since, as noted above, they are relied on to teach other features of the present invention.

Since Suzawa, Masumo, Takeuchi, Guldi, Wolf and Yanagisawa do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained.

Furthermore, with respect to independent claims 35, 37, 39, 40, 42 and 45, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Suzawa, Masumo, Takeuchi and Yanagisawa or to combine reference teachings to achieve the claimed invention.

The Official Action asserts that it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a resin material insulating layer over the silicon nitride interlayer insulating film (p. 8, Paper No. 20). However, Suzawa only discloses the silicon nitride interlayer insulating film. Also, Yanagisawa only discloses that a resin material insulating layer is used as the insulating film between the light shielding layer and the display pixel electrode. In contrast, as noted above, claims 35, 37, 39, 40, 42 and 45 recite the features of forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride, and forming a resin material layer over the interlayer insulating

film. Nothing in Suzawa and Yanagisawa teach or suggest why one with ordinary skill in the art would be motivated to form the polyimide organic insulation film of Yanagisawa on the interlayer insulating film 611 of Suzawa. Therefore, there is no motivation to combine Suzawa and Yanagisawa. Masumo and Takeuchi do not provide such motivation.

Even assuming motivation could be found, the Official Action has not given any indication that one with ordinary skill in the art at the time of the invention would have had a reasonable expectation of success when combining Suzawa, Masumo, Takeuchi and Yanagisawa.

The Applicants further contend that even assuming, *arguendo*, that the combination of Suzawa, Masumo, Takeuchi and Yanagisawa is proper, there is a lack of suggestion as to why a skilled artisan would use the proposed modifications to achieve the unobvious advantages first recognized by the Applicants. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 7 of the Official Action rejects claims 1-3 and 35-51 under the doctrine of obviousness-type double patenting over claims 1-38 of U.S. Patent No. 6,180,439 to Yamazaki et al. in view of Suzawa, Masumo, Takeuchi, Guldi, Wolf and Yanagisawa. As stated in MPEP § 804, under the heading "Obviousness-Type," in order to form an obviousness-type double patenting rejection, a claim in the present application must define an invention that is merely an obvious variation of an invention claimed in the prior art patent, and the claimed subject matter must not be patentably distinct from the subject matter claimed in a commonly owned patent. Also, the patent principally underlying the double patenting rejection is not considered prior art.

The Applicants respectfully traverse the obviousness-type double patenting rejection because independent claims 1 and 35-45 of the present invention are patentably distinct from the claims of Yamazaki '439, even in view of Suzawa, Masumo, Takeuchi, Guldi, Wolf and Yanagisawa. Specifically, the independent claims of the

present invention recite performing a plasma treatment to the semiconductor island and/or forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride, and forming a resin material layer over the interlayer insulating film. The claims of Yamazaki '439 do not teach or suggest these features of the present invention. For the reasons stated above, Suzawa, Masumo, Takeuchi, Guldi, Wolf and Yanagisawa do not teach or suggest the features of the present invention, either. The Applicants respectfully submit that the subject application is patentably distinct from the claims of the Yamazaki '439 patent. Reconsideration of the obviousness-type double patenting rejection is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1 and 35-45 as follows.

1. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning said semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween; and

forming at least a source region and a drain region in the semiconductor island,

wherein irradiation of laser light is performed after forming said semiconductor film.

35. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween; [and]

forming at least a source region and a drain region in the semiconductor island;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film.

36. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film by using mixed gases of TEOS and N_2O wherein the second gate insulating film comprises silicon oxide nitride; and

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween.

37. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film.

38. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning the semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film by using mixed gases of TEOS and N_2O wherein the second gate insulating film comprises silicon oxide nitride; and

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween.

wherein irradiation of laser light is performed after forming said semiconductor film.

39. (Amended) A method for manufacturing a semiconductor device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning the semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film,

wherein irradiation of laser light is performed after forming said semiconductor film.

40. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween; [and]

forming at least a source region and a drain region in the semiconductor island;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film.

41. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film by using mixed gases of TEOS and N_2O wherein the second gate insulating film comprises silicon oxide nitride; and

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween.

42. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor island on an insulating surface, the semiconductor island having a tapered shape, wherein the tapered shape has an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film.

43. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning said semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween; and

forming at least a source region and a drain region in the semiconductor island,

wherein irradiation of laser light is performed after forming said semiconductor film.

44. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning the semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film by using mixed gases of TEOS and N_2O wherein the second gate insulating film comprises silicon oxide nitride; and

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween,

wherein irradiation of laser light is performed after forming said semiconductor film.

45. (Amended) A method for manufacturing [a] an electroluminescence device comprising:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning the semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface;

performing a plasma treatment to the semiconductor island;

forming a first gate insulating film over the semiconductor island wherein the first gate insulating film comprises silicon oxide;

forming a second gate insulating film over the first gate insulating film wherein the second gate insulating film comprises silicon oxide nitride;

forming a gate electrode over the semiconductor island with the first gate insulating film and the second gate insulating film therebetween;

forming an interlayer insulating film over the gate electrode wherein the interlayer insulating film comprises silicon nitride; and

forming a resin material layer over the interlayer insulating film,

wherein irradiation of laser light is performed after forming said semiconductor film.